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Design and Performance Analysis of Interface Circuits in Hybrid Input Energy Harvesting for Semi-Active RFID Tag

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This paper presents a hybrid input energy harvesting system that combines RF and thermal energy sources in parallel to produce adequate DC voltage to replace the battery as a partial source of the semi-active RFID tag and supply it with the energy harvested from the proposed system. The proposed RF-DC Dickson's rectifier and DC-DC converter circuit topologies based on voltage multiplier and ultra-low power design are presented to enhance the performance of the hybrid system especially when the harvesters are operating at minimum input level. The entire system is designed using a standard 0.13 um CMOS technology, and is simulated to handle input voltages as low as 40 mV peak from RF harvester and 140 mV for thermal harvester. The simulated results show the proposed system can generate a minimum output voltage of 1.40 V from the -18 dBm single-source RF harvester with 2 MΩ load resistance. Meanwhile, a 6.35 V can be generated at a maximum combined configuration of -10 dBm RF input power and 10 ˚C temperature difference. These shown that the proposed hybrid system is able to produce sufficient output DC voltage to replace the battery as a partial source of the semi-active RFID tag and supply it with the energy provided.

Keywords: energy harvesting; RFID tag; hybrid input; RF-DC rectifier; DC-DC converter

I. INTRODUCTION

In recent years, the growing uses of radio frequency identification (RFID) systems, especially in biomedical, industrial, military and security applications (Mohamad *et al.*, 2017) has increased the importance of the power supply generation and the lifespan of the RFID tag devices. Nonetheless, this is not a big deal for the passive RFID tags as it gets operating power solely from a radio frequency (RF) signals transmitted from RFID reader to generate the tag responses (Oh *et al.*, 2012). On the other hand, for semi-passive and active tags that use integrated battery as a partial or sole power source for the tag circuitry (Bakhtiar *et al.*, 2010), their major drawback is their limited lifespan issues. Even though the tags can be powered by the battery and RF energy transmitted from the RFID reader but once the battery died, the tag cannot be fully activated. Frequent use of the tags will shorten the battery lifespan. Ongoing maintenance to charge and replace the battery is not easy as it involves a large amount of tags and waste in terms of time and maintenance costs. Thus, one of the practicable solutions is to utilize the advantages of the energy harvesting technology.

Nowadays, many researchers come out to design multi-input energy harvesting systems that combine more than one energy source to enhance the reliability and functionality of the overall system. Several combinations and design techniques have been reported in the literature. Tan and Panda have presented energy harvesting from two energy sources, i.e., thermal energy from machines heat and ambient light energy from artificial lighting. These two energies are combined using one power management circuit to enhance the performance of indoor wireless sensor nodes over lifetime

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(Tan *et al.*, 2011). Chang and Lee have extended their thermoelectric energy harvesting system by combining it with RF energy sources to obtain maximum output power extraction (Chang & Lee, 2016). In order to overcome the threshold-voltage limitation of the RF input signal in RFID sensor, Nguyen *et al.* have proposed to add piezoelectric transducer as secondary power source (Nguyen *et al.*, 2014). In another approach, Sampe *et al.* have combined three input energy harvester which are thermal energy, RF and vibration to produce sufficient output voltage to power the biomedical devices (Sampe *et al.*, 2017). Regardless of the combinations and design techniques, the real challenges are the system has to deal with a wide range of input voltages and different characteristics of source impedances for different harvesters (Bandyopadhyay & Chandrakasan, 2012).

In this paper, we proposed an architecture of hybrid input energy harvesting system that combines two input energy sources: RF signal and thermoelectric generator (TEG) based on the published design by (Chang & Lee, 2016) with major modifications. Figure 1 shows the post-layout of their design which can deliver the output voltage of 1.8 V and maximum output power of 36 mW. The design is implemented in a 40 nm CMOS technology and occupies the active layout area of 0.46 mm².

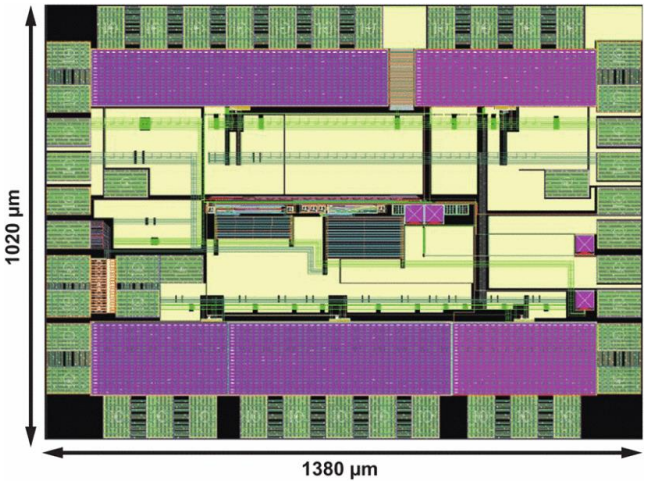

Figure 1. Layout of the multi-source energy harvesting system (Chang & Lee, 2016)

In our previous work (Mohamad *et al.*, 2018), a maximum output DC voltage of 3.44 V, 1.19 V and 3.40 V can be harvested from the maximum input level of RF, thermal and combination of both sources respectively. But for minimum input level, the output voltage is still too low to reach the minimum level of the battery operating voltage. Thus, in this work, the proposed system is reconfigured with RF-DC Dickson's rectifier and DC-DC converter interface circuit architecture to further increase the output voltage to suit the semi-active tag's battery supply voltage.

In our approach, the system is designed to handle input amplitude as low as 40 mV for RF signals (AC voltage) and 140 mV for thermal (DC voltage) respectively. The main objective is the proposed system can extract adequate voltage either from RF or TEG harvester individually or both harvesters simultaneously. The block diagram of the new proposed system architecture is shown in Figure 2.

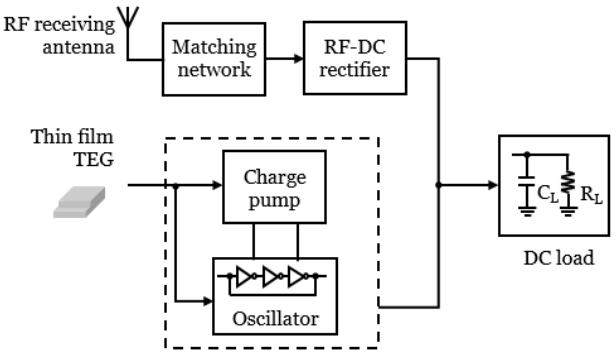

Figure 2. Block diagram of the proposed hybrid input energy harvesting system

The rest of the paper is structured in three main sections. In Section II, the proposed architecture for the RF, thermal and hybrid system is presented in detail here. Section III demonstrates the simulation results and analysis of the proposed system. Finally, conclusions are provided in Section IV.

II. SYSTEM ARCHITECTURE

The equivalent electrical circuit of the hybrid input energy harvesting systems is illustrated in Figure 3. RF and thermal energy harvesters are combined using an on-chip inductor and are directly connected to the storage capacitor C_L and load resistance R_L. For preventing the reverse-biased current from flowing back to the interface circuits, two diode-connected PMOS transistors (M13 and M46) are added at each energy harvester's output terminal.

RF-DC rectifier and a low startup voltage DC-DC converter are required to interface between RF and TEG harvesters and the load. Since the output voltage from the RF and thermal energy sources are very low in the range of a few millivolts, those voltages must be increased to the required level before

being supplied to the load. To solve this problem, circuit topology based on the voltage multiplier is introduced in the design. For the performance analysis, several simulations in terms of input voltage and load resistance variations have been performed for both harvesters, individually and simultaneously.

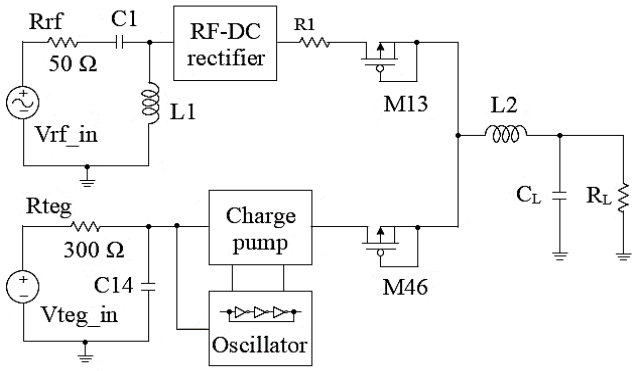

Figure 3. Equivalent electrical circuit of the proposed RF and thermal hybrid input energy harvesting system

A. RF Energy Harvesting System

As illustrated in the Figure 2, the proposed RF energy harvester system consists of a matching network and a rectifier. The unused and undesirably radiated RF signals from the RFID reader or in the environment is first being harvested by the antenna. Then, RF-DC rectifier is required to convert the received AC voltage signal to a DC voltage to supply the required DC power for the device. For ultra-high frequency (UHF) RFID applications, the operating frequency is in the range of 860 – 960 MHz (Worldwide EPC compliant). For the simulation purpose, a 915 MHz ultra-high frequency (UHF) signal, 50 Ω input impedance and input power range of -18 dBm (40 mV_{peak}) to -10 dBm (100 mV_{peak}) is assumed at the source.

In RF energy harvesting, an impedance matching circuit is required at the interface with the antenna to boost its low input voltage to be larger than the threshold voltage (V_{th}) of MOS transistors (Sampe *et al.*, 2016; Yunus *et al.*, 2017). For instance, in this design the input voltage can be boosted to 521 mV_{peak} under an input power of 100 μW. To ensure for maximum power trasfer to the matched rectifier, inductor-capacitor (LC) matching circuit is designed to match the input impedance of the rectifier to the 50 Ω output impedance of the antenna (Sampe *et al.*, 2017; Yunus *et al.*, 2018; Yunus *et al.*, 2019).

Throughout decades of studies, a lot of research on the RF-DC rectifiers have been done to improve the efficiency and sensitivity values of the RF energy harvesting system (Asli & Wong, 2018; Chouhan & Halonen, 2014; Dai *et al.*, 2015) . Several topologies have been proposed such as implementation using a Schottky diode (Marshall *et al.*, 2015; Nimo *et al.*, 2012) and CMOS transistor (Dastabian *et al.*, 2017; Nimo *et al.*, 2012; Shokrani *et al.*, 2012). As for RFID applications, a CMOS rectifier topology is preferred due to cost and design limitations of the tag (Oh & Wentzloff, 2012). In this work, RF-DC rectifier based on the voltage multiplier circuit topology has been used to convert the RF input signal and increase the output voltage to the desired value. The voltage multiplier circuit is formed by cascading a 6-stage RF-DC Dickson's rectifier as shown in Figure 4. This topology design is chosen to minimize the overall architecture sensitivity and to achieve a better efficiency (Pasca *et al.*, 2015). Moreover, the small width to length (W/L) ratio of the transistors has been used to achieve the target output voltage in the simulation input power range.

In this design the output of the N-stage rectifier is connected to the N+1 stage rectifier. Each stage comprises of two capacitors and two diode-connected NMOS transistors. For better performance of the diode-connected NMOS transistor, the bulk modulation technique is applied in the design. This is done by connecting the bulk to the drain which improves the rectifier output voltage by reducing the threshold voltage and leakage current of the transistor (Shokrani *et al.*, 2012).

Theoretically, when V_{rf_in} is in a negative cycle, the odd number of NMOS diodes i.e. M1, M3, M5, etc will turn ON and the even number of NMOS diodes i.e. M2, M4, M6, etc will turn OFF. Thus, the current will flow into capacitor C2 and charge it to V_{rf_in}, C4 to $3V_{rf\_in}$ and so on. Contrarily, when V_{rf_in} is in a positive cycle, the odd number of NMOS diodes will turn OFF and the even number of NMOS diodes will turn ON. The capacitor C3 will charge to $2V_{rf\_in}$, C5 will charge to $4V_{rf\_in}$ and so on. Thus, the output DC voltage of N stages of Dickson's rectifier can be expressed by using an equation

$$V_{rf\_dc} = 2N \cdot V_{rf\_in} \quad (1)$$

where V_{rf_in} is the peak voltage of the RF input signal after impedance matching circuit. However, when a load is connected to the output of the rectifier and since there will be a voltage drop across the diode-connected NMOS transistor, V_{DROP}, equation (1) will become

$$V_{rf\_dc} = 2N \cdot (V_{rf\_in} - V_{DROP}) - I_L \cdot R_r \quad (2)$$

where I_L is the load current and R_r is the rectifier output resistance.

B. Thermal Energy Harvesting System

Thermal energy harvester is employed for transforming heat energy into electricity when there is a temperature difference between the hot side and cold side through a phenomenon called the Seebeck effect (Bhatnagar & Owende, 2015; Jalil & Sampe, 2016; Mohamad *et al.*, 2017; Suzuki & Deng 2016). Electrically, the TEG module can be modelled as a DC voltage source, Vteg_in in series with an internal resistance, Rteg as shown in Figure 3. The open-circuit voltage can be expressed as

$$V_{TEG(OC)} = S.\Delta T \quad (3)$$

where S represent the Seebeck coefficient of the thermoelectric material and ΔT is the temperature difference applied to each side of the device. The voltage produced is proportional to the ΔT (Jfri *et al.*, 2015; Ramadass & Chandrakasan, 2011).

As illustrated in Figure 3, the output voltage from the TEG harvester Vteg_in is applied to low startup voltage DC-DC converter consists of a charge-pump and oscillator circuits. The cross-coupled charge pump with internal start-up is used in the design to provide a further step-up of the Vteg_in voltage. The proposed circuit is formed based on the voltage multiplier technique by cascading 4-stage cross-coupled circuit (Figure 5) driven by an oscillator clock signals. Each stage consists of two NMOSs, two PMOSs and two pumping capacitors.

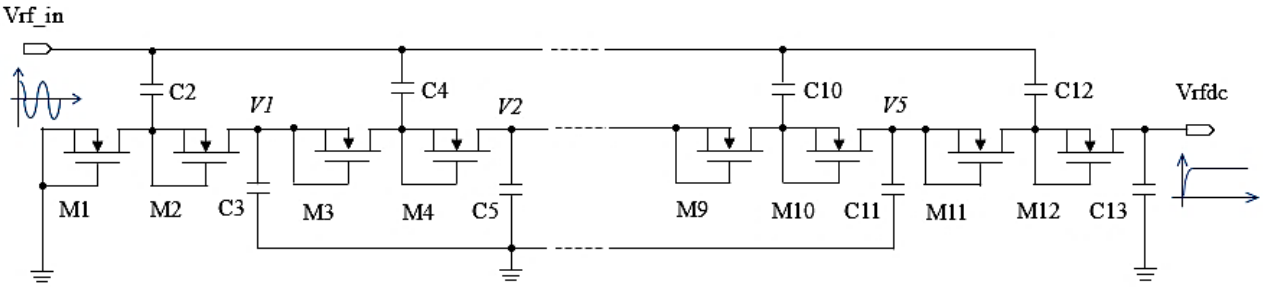

Figure 4. The proposed 6-stage RF-DC Dickson's rectifier of the RF energy harvesting circuit

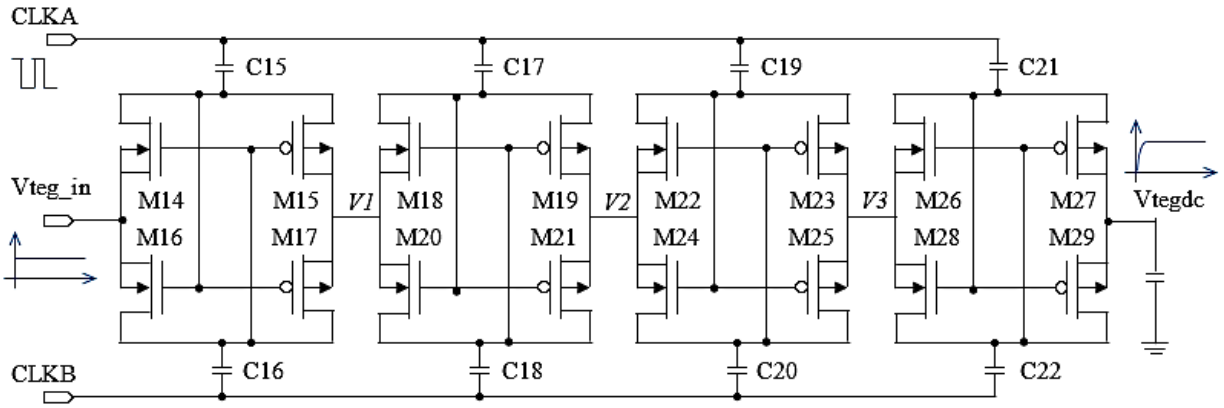

Figure 5. The proposed 4-stage cross-coupled charge pump circuit based on the voltage multiplier structure

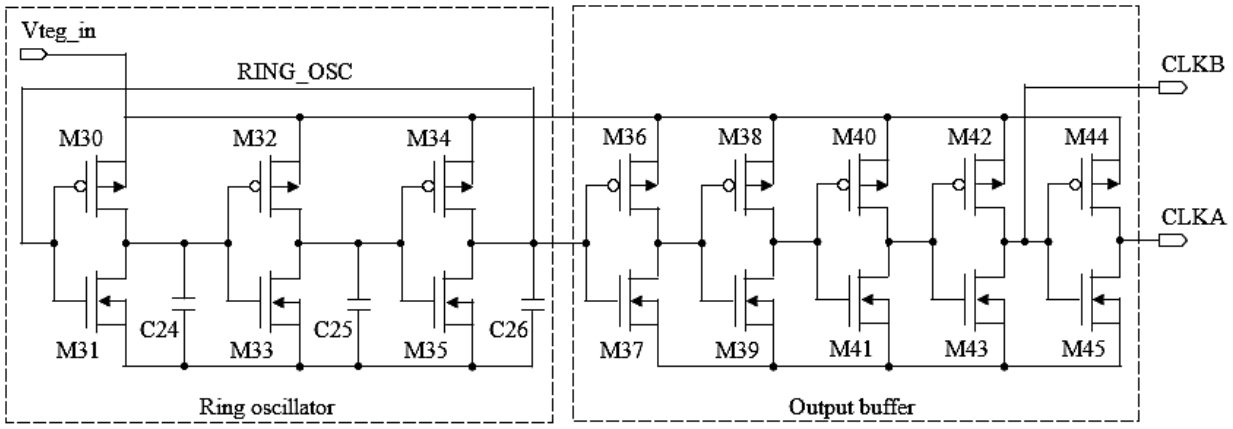

Figure 6. 3-stage ring oscillator with five inverter-based buffers circuit

As shown in Figure 6, 3-stage ring oscillator with five inverter-based buffers circuit are used to generate two out of phase clock signals, CLKA and CLKB which have peak-to-peak voltage of Vteg_in. The design is based on a low-voltage and low-power oscillator introduced by Ashraf and Masoumi. Minimum number of stages are used to generate high-frequency clock-signals need by charge-pump to rapidly charge the output capacitor (Ashraf & Masoumi, 2016). A buffer circuit helps for level shifter and make the clock output smoother. Large size of buffers also improve the clock output swing and the current drivability (Peng *et al.*, 2014). For design optimization, small W/L ratio of the CMOS transistors is used to lower the V_{th} and minimize the power consumption.

III. RESULTS AND DISCUSSIONS

The proposed hybrid input energy harvesting system has been designed and simulated based on a standard 0.13 µm CMOS technology and the characteristics given in Table 1. To study the harvester system's performance, it is simulated by varying the harvester input voltage level and the load resistance. Then, the minimum and maximum output DC voltage, V_{DC} and the output power harvested, P_{OUT} of each harvester and the combination of them are measured and recorded for each simulation setting. As a design guide, the battery operating voltage of the semi-active tag is considered between 1.25 V and 3.65 V, and the average battery current value during the wakeup state is below 10 µA.

In this proposed design, thermal energy harvesting is simulated based on the characteristics of Micropelt thin film TEG module MPG-D751 (Micropelt). This new generation TEG has a smaller product size with dimensions of 3.36 x 4.25 mm2 (Micropelt, GmbH). The characteristics of the module are summarized in Table 1.

Table 1. Characteristics of RF harvester and thermal harvester

RF harvester	
Input frequency	915 MHz
Input impedance	50 Ω
Input power range	-18 dBm ~ -10 dBm ($40\ mV_{peak}$ ~ $100\ mV_{peak}$)
Thermal harvester	
Module	Micropelt MPG-D751
Operating range	ΔT = 1 °C ~ 10 °C
Electrical resistance	300 Ω
Seebeck voltage	140 mV/°C
Open circuit voltage	0.14 V ~ 1.4 V
Maximum power harvested	16.3 µW ~ 1.63 mW

A. Single Input Energy Harvesting from RF Energy Source

The proposed RF energy harvesting circuit is simulated at 915 MHz input frequency with voltage varying from 40 mV_{peak} to 100 mV_{peak}. For RF-DC Dickson's rectifier design optimization, the size of NMOS transistors with W/L ratio of 10 µm/0.13 µm and 10 pF for coupling capacitors are

implemented through simulation. Figure 7 shows the simulated output power harvested, P_{OUT} as a function of output DC voltage, V_{DC} at various RF input level, RF_{IN}. At this operation condition, there is no input source from the thermal energy harvester. From the plotted graph, the maximum output DC voltage, V_{DCmax} and the maximum output power harvested, P_{OUTmax} are 2.79 V and 1.07 µW, respectively at minimum RF_{IN} = -18 dBm. V_{DCmax} and P_{OUTmax} values increase accordingly when RF input level increases. V_{DCmax} is measured when the circuit is not connected to any load and no current at the output which represents the open-circuit voltage for each RF_{IN}. For maximum RF_{IN} = -10 dBm, the V_{DCmax} = 7.28 V and P_{OUTmax} = 10.68 µW.

Figure 8 shows V_{DC} as a function of RF_{IN}. When R_L increases, the V_{DC} increases accordingly. From the figure shown, it can be observed that when R_L = 2 MΩ, a minimum V_{DC} of 1.40 V and a maximum of 3.87 V is able to be generated at RF input level -18 dBm and -10 dBm respectively. These minimum and maximum output voltages can accommodate the battery operating voltage of the semi-active RFID tag which in the range of 1.25 V - 3.65 V.

B. Single Input Energy Harvesting from Thermal Energy Source

In the situation when there is only thermal energy source available in the system, the performance of the system is studied by varying the temperature differences, ΔT and load resistances, R_L. Referring to Figure 9, it can be seen for various values of ΔT between 1 - 10 °C, the V_{DCmax} and P_{OUTmax} are increased correspond to ΔT. For example, when ΔT = 5 °C: V_{DCmax} = 3.42 V, P_{OUTmax} = 12.89 µW, and ΔT = 7 °C: V_{DCmax} = 4.77 V, P_{OUTmax} = 34.21 µW, etc.

Figure 10 shows the output DC voltages as a function of ΔT. V_{DC} increases linearly with the increases in ΔT and R_L. As shown in the figure, the thermal energy harvester must operate at least at ΔT = 3 °C and R_L = 2 MΩ to achieve the minimum battery operating voltage. Meanwhile, the harvester must operate at ΔT = 6 °C for the same R_L value to achieve the maximum battery operating voltage.

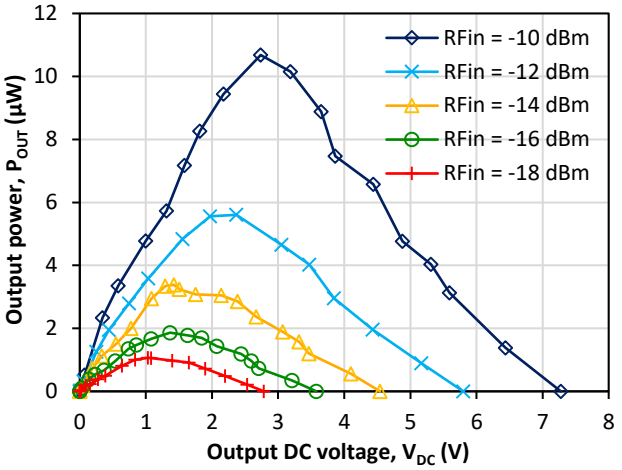

Figure 7. P_{OUT} versus V_{DC} of RF energy source for various RF input level

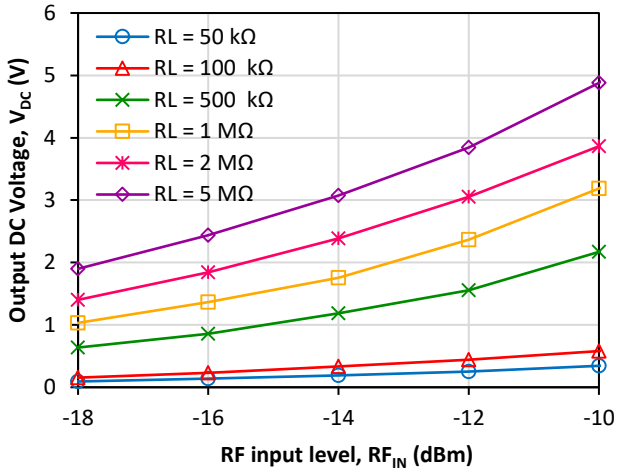

Figure 8. V_{DC} versus RF_{IN} of RF energy sources at different load resistance, R_L

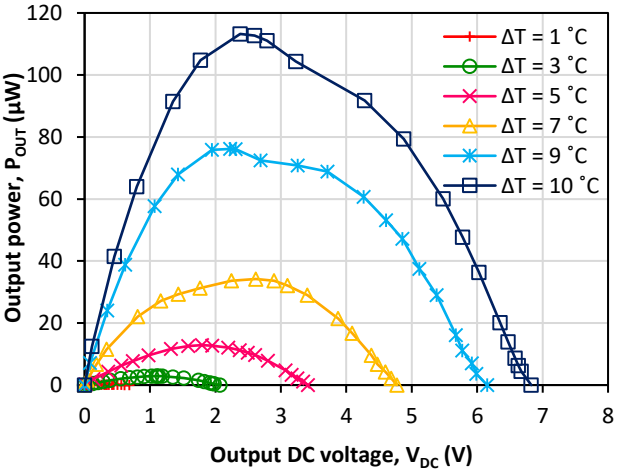

Figure 9. P_{OUT} versus V_{DC} of thermal energy source for various temperature differences

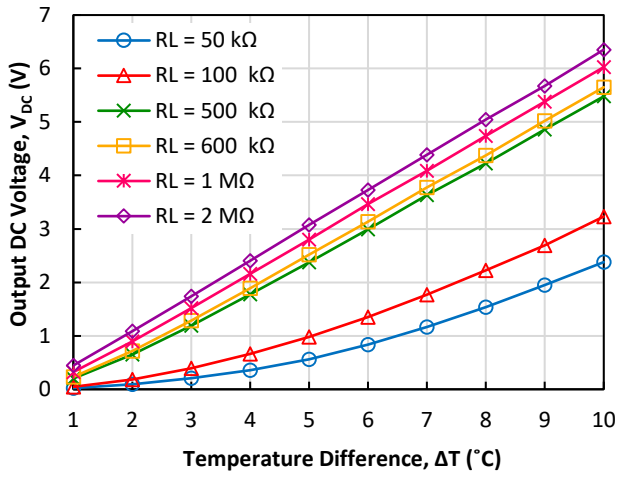

Figure 10. V_{DC} versus ΔT of thermal energy source at different load resistances

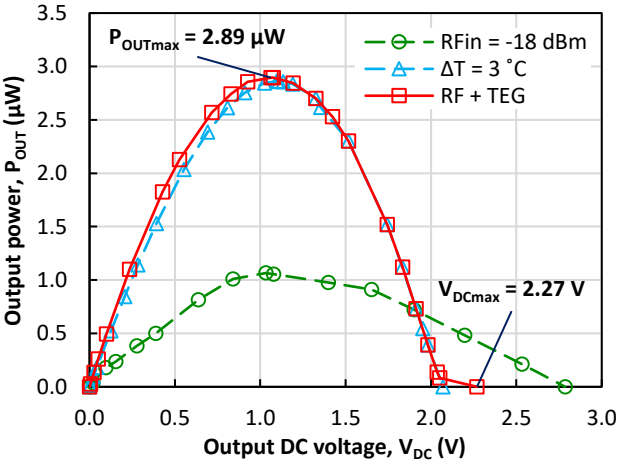

Figure 11. P_{OUT} versus V_{DC} of a hybrid input energy harvesting system under the minimum input level RF_{IN} = -18 dBm and ΔT = 3 °C

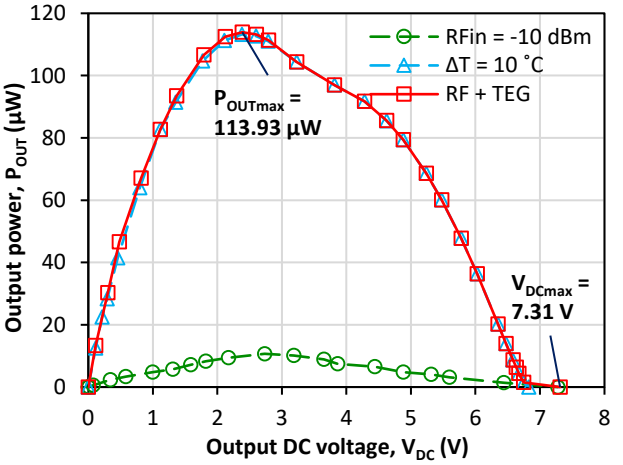

Figure 12. P_{OUT} versus V_{DC} of a hybrid input energy harvesting system under the maximum input level RF_{IN} = -10 dBm and ΔT = 10 °C

C. Hybrid Input Energy Harvesting from RF and Thermal Energy Source

Figure 11 show the power curves of the hybrid input energy harvesting system under the minimum level of RF (RF_{IN} = -18 dBm) and thermal (ΔT = 3 °C) energy sources when they are harvested simultaneously. The simulated results show that the system can generate a maximum power of 2.89 µW. The maximum available output DC voltage is 2.27 V. Referring to these figures, it can be observed that P_{OUT} of the hybrid input energy harvesting (RF + TEG) is higher than P_{OUT} of the single input energy harvesting for V_{DC} < 1.33 V. However, P_{OUT} (RF + TEG) is equal to P_{OUT} (TEG) when V_{DC} > 1.33 V. The reason is that when V_{DC} (RF + TEG) is greater than Vrfdc, the RF harvester will operate in the open-circuit mode and only TEG power is harvested.

Likewise, for the hybrid input energy harvesting system under the maximum level of RF (-10 dBm) and thermal (ΔT = 10 °C) energy sources, the simulated power curves are shown in Figure 12. The system can generate a maximum available output DC voltage of 7.31 V and a maximum power of 113.93 µW. P_{OUT} (RF + TEG) is slightly increased for V_{DC} (RF + TEG) < 3.23 V, whereas P_{OUT} (RF + TEG) is equal to P_{OUT} (TEG) when V_{DC} (RF + TEG) ≥ Vrfdc.

Table 2 summarizes the simulated results obtained from the proposed energy harvesting system when individual input as well as hybrid input under 2 MΩ resistive load is presented.

Table 2. Optimum output values harvested from the proposed RF and thermal hybrid input energy harvesting system when R_L = 2 MΩ

	V_{DC}		P_{OUT}	
Active Energy Harvesters	**Min.**	**Max.**	**Min.**	**Max.**
RF (-18 dBm ~ -10 dBm)	1.40 V	3.87 V	0.98 µW	7.47 µW
TEG (ΔT = 3 °C ~ 10 °C)	1.74 V	6.35 V	1.52 µW	20.17 µW
RF + TEG	1.74 V	6.35 V	1.52 µW	20.18 µW

IV. CONCLUSION

This paper presents a hybrid input energy harvesting system combining RF and thermal energy harvesters for ultra-low power semi-active UHF RFID tags. The architecture is designed based on 0.13 µm CMOS technology and simulated using PSpice software. From the simulation results, it shows that the proposed system with improved interface circuits design able to generate output DC voltage in the range of 1.40 V – 6.35 V for single input energy harvester and 1.74 V – 6.35 V for hybrid input energy harvester under 2 MΩ resistive load. These shown that when the system is operated either as a single input source or hybrid input source, it able to accommodate the tag's battery operating voltage which in the range of 1.25 V – 3.65. For a more accurate verification of the proposed design performance, a post-layout simulation will be carried out in future work.

V. ACKNOWLEDGEMENT

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