ASM Sc. J., 17, 2022

https://doi.org/10.32802/asmscj.2022.948

High Conversion Gain Self-Oscillating Mixer for 5G mm-wave Applications

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We develop in this paper, a high conversion gain self-oscillating mixer (SOM) for 5G mm-wave applications using commercial 0.15µm GaAs PHEMT from UMS foundry. The up-conversion SOM transpose the IF signal from 2 GHz to 26 GHz LSB (lower sideband) signal using a 28GHz LO signal. The simulation results show that the SOM has a maximum conversion gain of 19dB, according to our knowledge, this structure presents the highest gain compared to SOMs published in the literature. While the 1dB compression point is obtained for an IF power of -20.6 dBm. The SOM circuit consumes 129mW and it occupies an area of 0.741 mm².

Keywords: Cascode cell; mm-Wave band; pHEMT mixer; Self-Oscillating Mixer

I. INTRODUCTION

Thanks to the performance evolution of the circuit manufacturing processes, as well as the evolution of the design methods of Monolithic Microwave Integrated Circuit (MMIC), the recently designed and published transmission and reception system blocks, have shown very satisfactory and promising performances (Zhou *et. al.,* 2020; Es-saqy *et. al.,* 2020a; Hamada *et. al.,* 2020; Nam, 2020; Gao, 2020). In recent years, numerous publications describing MMIC mixers, suitable for mm-wave applications, have been published (Hamada *et. al,* 2020; Gao *et. al.,* 2020; Chen *et. al.,* 2020; Wang *et al.,* 2019). Although the combination of a local oscillator is essential for the operation of the mixer, whether at up- or down-conversion. However, in most of published papers in the literature, the authors deal either with the mixer circuit (Gao *et. al.,* 2020; Chen *et. al.,* 2020; Faitah *et. al.,* 2009; Hurskainen *et. al.,* 2020; Aye *et al.,* 2014) or the local oscillators (Wen *et. al.,* 2005; Es-saqy *et. al.,* 2020b; Li *et. al.,* 2020; Wang & Chen, 2020; Shehata *et. al.,* 2019; Sakka *et. al.,* 2020; Iotti *et al.,* 2017).

In this paper, we propose the study and design of a Self-Oscillating Mixer (SOM) which combine, simultaneously, the harmonic generation and frequency conversion functions in a single circuit (Figure 1(b)). The proposed up-converter SOM converts an IF signal of 2 GHz to a LSB (low-sideband) signal of 26 GHz, using a 28 GHz LO signal. The integration of these two blocks, indispensable for RF signal transmission systems, allowing the development of small size, low manufacturing costs and power consumption chip (Winkler *et al.,* 2007), as well as minimising the parasitic inductance brought by bonding wires (Sun *et al.,* 2020).

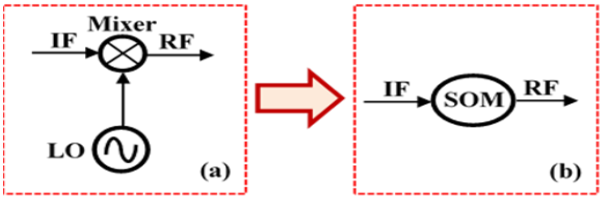

Figure 1. (a) LO and Mixer, and (b) Self-Oscillating Mixer SOM

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In the paper Winkler *et al.* (2007), the authors propose a Self-Oscillating Mixer based on the use of the sub-harmonic method, i.e., instead of mixing the incident signal with the fundamental of the LO frequency, the third harmonic of the LO frequency is used (Winkler *et al.,* 2007). The operating frequency of this SOM is 5.8 GHz with a conversion gain of 11.1 dB. While in the paper Ke and Chiu (2012), the authors propose a SOM based on the CMOS transistor, for millimetre frequencies, around 60 GHz, the conversion gain is about 3.4 dB, the area occupied by the circuit, without pads, is 0.64 mm² (Ke & Chiu, 2012). Except for the SOM proposed in Winkler *et al.* (2007), whose gain exceeds 11 dB, most of the SOMs published in the literature have a gain lower than 6 dB (Ke & Chiu, 2012; Al-Ayed, 2015; Pal & Mandal, 2018).

Table 1. Typical data of the pHEMT transistor

Parameter	**Typical value**
Power density	300 mW/mm
Gate length	0.15 µm
$Ids_{saturation}$	550 mA/mm
Cut off frequency f_T	110 GHz
V_{pinch}	-0.7 V
G_m(Max)	640 mS/mm
Noise	0.5dB @ 10GHz 1.9dB @ 60GHz
Gain	14dB @ 10GHz 6dB @ 60GHz

The relatively high conversion gain for simple mixers, between 4 and 8 dB in (Xu *et. al.,* 2000; Wang *et al.,* 2019), makes them more attractive for millimetre-wave applications, where LO power is generally low; about of -7 dBm, -3.5 dBm or 0 dBm for the local oscillators designed by the authors of papers from Fu *et al.* (2020), Li and Cheng (2020) and Es-saqy *et al.* (2021), respectively (Fu *et. al.,* 2020; Li & Cheng, 2020; Es-saqy *et al.,* 2021). Nevertheless, these structures present a very low level of isolation between their three ports and, thus, require the use of filter circuits at each port.

In this paper, we design a SOM, using cascode cell which has natural isolation between the two input ports, i.e., LO-to-IF and IF-to-LO. The designed SOM has a maximum conversion gain of 19dB. According to our knowledge, this is the highest gain compared to SOMs published in the literature.

This paper is organised as follows. In section 2, we designed the mixer using the pHEMT cascode cell. The third section is dedicated to the Voltage Controlled Oscillator design. While the fourth section presents the circuit of the SOM and the simulation results. Then we conclude in the section V.

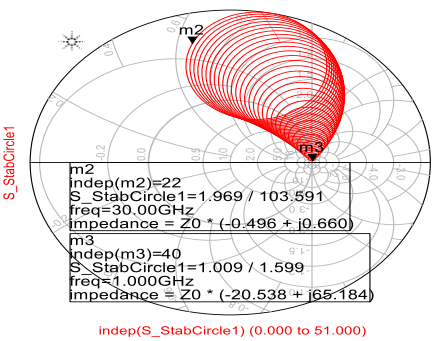
II. MIXER WITH PHEMT CASCODE CELL

A. pHEMT Transistor

Firstly, we will study the active component of the circuit by detailing the physical and electrical characteristics of the used transistor. Then for the design of our mixer, a pHEMT transistors with low noise and high gain is chosen. The circuit will be designed using PH15 technological process of the UMS foundry, its technological and physical properties are presented in Table 1. The selected transistor has a gate length L = 0.15 µm, a gate width W=30 µm, and one finger gate number.

(a)

(b)



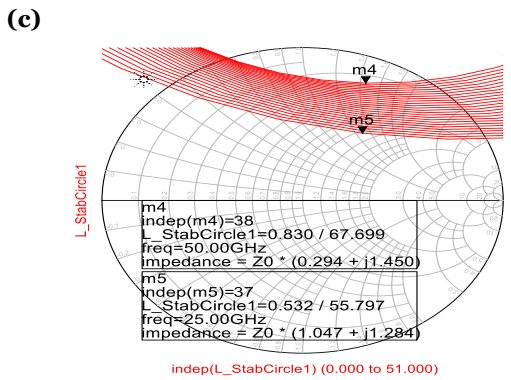
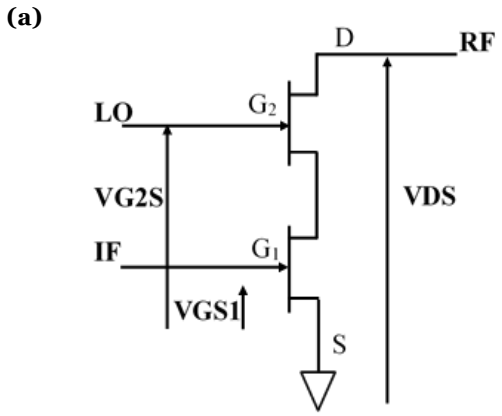


Figure 2. pHEMT stability factor K (a), stability circles at the transistor input (b) stability circles at the transistor output (c)

To avoid the phenomenon of oscillation, studying the stability of the pHEMT transistor is the first step in the design of a mixer. According to Figure 2(a), the stability factor has a positive value and less than 1 in the frequency range between 1 and 50 GHz. This implies that the transistor understudy is conditionally stable. Therefore, a separate stability study must be carried out at the transistor input and output. The stability circles (Figure 2(b) and (c)) show that the impedances making the input/output stable form most of the Smith chart, therefore we can conclude on the stability of the transistor. The transistor gates will be excited by the 2 GHz IF signal and by the 28 GHz LO signal, for this, the input stability is verified over the frequency range from 1 to 30 GHz. Then the output stability is studied over the band from 25 to 50 GHz (the frequency of the output signal will be 26 GHz).



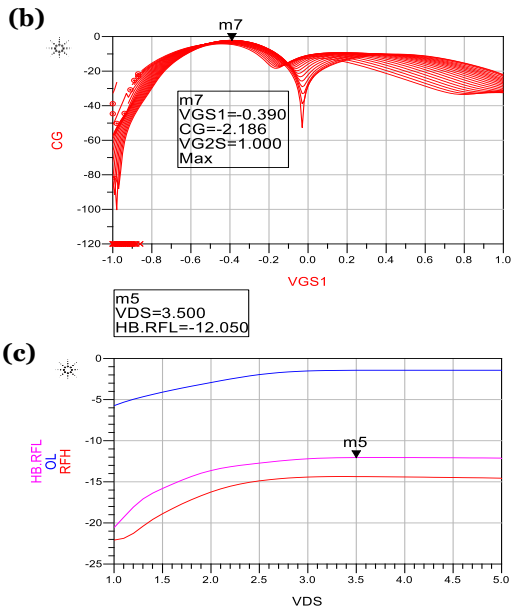


Figure 3. (a) Electrical circuit of the cascode cell, (b) Conversion gain variation of the cascode cell as a function of VGS1 for different values of VG2S (for VDS=3 V, IF_power=-10 dBm, and LO_power=5 dBm), and (c) Variation of the LO, RFL, and RFH output powers as a function of the VDS voltage (for VG2S=1 V, VGS1=-0.4 V, IF_power=-10 dBm and LO_power=5 dBm)

B. pHEMT Cascode Cell

The cascode cell is composed by two pHEMT transistors, where the source of one is connected to the drain of the other. One of the two pHEMT transistors operates in the linear region, while the second must operate in the non-linear region. In the case of up-conversion, the IF and OL signals are injected on both gates of the cascode system, however, the RF signal is extracted from the drain of top transistor (Figure 3(a)). The cascode cell is biased by three voltage sources VDS, VG2S, and VGS1.

Figure 3(b) shows the variation of the conversion gain as function of VG2S and VGS1. It shows that the optimal values of these two voltages are VG2S=1 V and VGS1=-0.4 V. In order to choose the optimal value of the VDS voltage, which corresponds to a maximum conversion gain, the variation of the LSB, USB (Upper sideband) and OL signal power as a function of VDS is plotted. The graph in Figure 3(c) shows that the three signals reach their maximum values for VDS voltages higher than 3.5 V, for this, we have chosen the value VDS=4 V. For all simulations performed in the following

paper, the values of the bias voltages VG2S, VGS1, and VDS are 1, -0.4, and 4 V respectively.

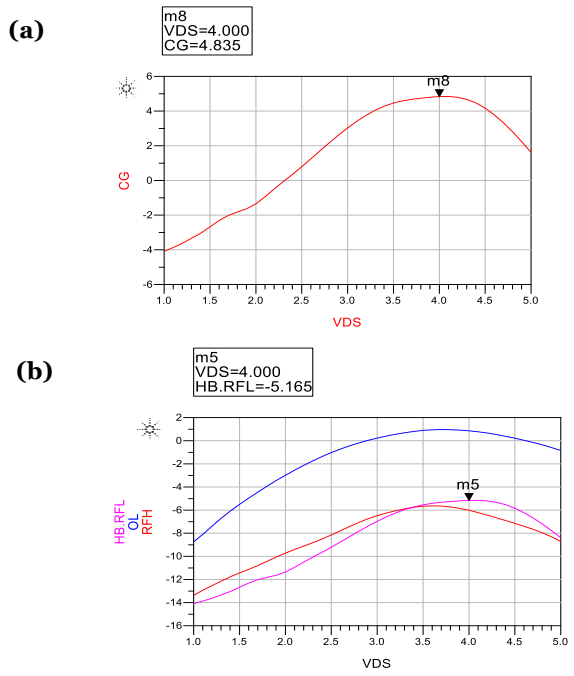


Figure 4. (a) Conversion gain variation of the cascode cell as a function of VGS1 for different values of VG2S (for VDS=3 V, IF_power=-10 dBm and LO_power=5 dBm), and (b) variation of the LO, RFL and RFH output powers as a function of the VDS voltage (for VG2S=1 V, VGS1=-0.4 V, IF_power=-10 dBm and LO_power=5 dBm), after insertion of the matching circuits

In order to improve the isolation between the different accesses of the cascode cell, and to improve its conversion gain, a matching network is inserted at the IF and RF accesses of the cascode cell. The simulation results show that the matching networks has increasing the LSB power by 7dB, i.e., from -12.05 dBm (Figure 3(c)) to -5.1 dBm (Figure 4(b)). Thus, the conversion gain increases also by 7 dB (from -2.2 dB before matching to 4.8 dB after matching).

After matching the circuit, we perform a stability study of the cascode cell, this is done using the S-parameters under Agilent's ADS software. Figure 5 shows the three reflection coefficients of the three cascode cell ports. S11 corresponds to the reflection coefficient of the LO port, whose LO signal frequency is around 28 GHz, S22 and S33 correspond to the reflection coefficients at the IF and RF ports, respectively.

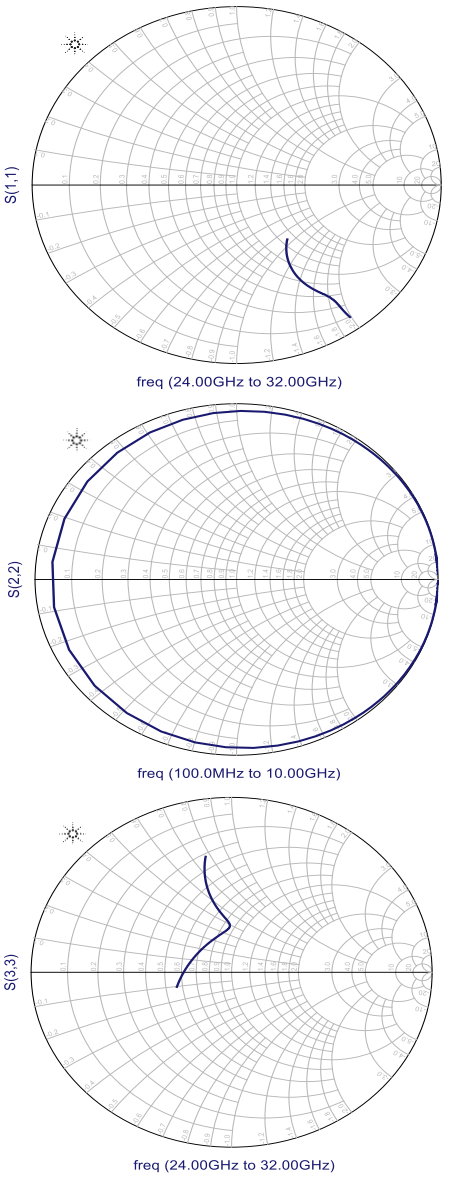


Figure 5. Reflection coefficients of the ports of the cascode cell, S11, S22 and S33 at the port LO, IF and RF, respectively These three responses are well contained in the Smith chart, which means that all the impedances forming these curves are positive real part impedances.

III. VOLTAGE CONTROLLED OSCILLATOR DESIGN

The use of low oscillation frequency VCOs requires the addition of a frequency multiplier, and even two frequency multipliers in some cases (Nam *et. al.,* 2020; Hurskainen *et al.,* 2020). This increases the complexity of the system and makes the occupied area and the manufacturing costs of the circuit higher. Therefore, in this section, we present the electrical circuit (Figure 6(a)), and some simulation results, of a voltage-controlled oscillator designed for 5G

applications, suitable for integration with our mixer to design a self-oscillating mixer. The oscillation frequency of this VCO varies between 26.46 and 28.9 GHz (Figure 6(d)), with a high output power exceeding 5 dBm (Figure 6(b)), as well as a low phase noise level of -113 dBc/Hz at an offset frequency of 1MHz (Figure 6(c)). This circuit is studied in detail in paper of Es-saqy *et al.* (2020a) and the design method is presented in paper of Es-saqy *et al.* (2021) (Es-saqy *et. al.*, 2020a; Es-saqy *et al.,* 2021).

IV. 5G MM-WAVE SELF-OSCILLATING MIXER (SOM)

After having detailed the two parts of the self-oscillating mixer, we will, in this section, describe the design phase of this device by integrating the two sub-circuits presented previously, as well as optimising the performance of the entire circuit. The integration of these two essential blocks for the RF signal transmission system will permit increasing the performance of the system in terms of cost and manufacturing time, as well as, minimising energy consumption and noise due to parasitic elements. The final size of the self-oscillating mixer, whose layout is shown in Figure 7, is 0.741 mm², with a length of 678 µm and a width of 1093 µm. Figures 8(a), (b) and (c) show the power spectrum present at the three ports of the self-oscillating mixer, from these simulation results we can deduce the isolations values between the different accesses (Table 2). The LO-to-IF, RF-to-IF and RF-to-LO isolations are respectively 50.3 dB, 62.3 dB and 16.48 dB. Thus we can conclude that this structure present a high isolation level. However, Figure 8(c) shows the conversion gain CG variation, versus the IF power. From this graph we can deduce that the maximum value of the CG is higher than 19 dB and the compression point at 1 dB is obtained for an IF power value of -20.6 dBm.

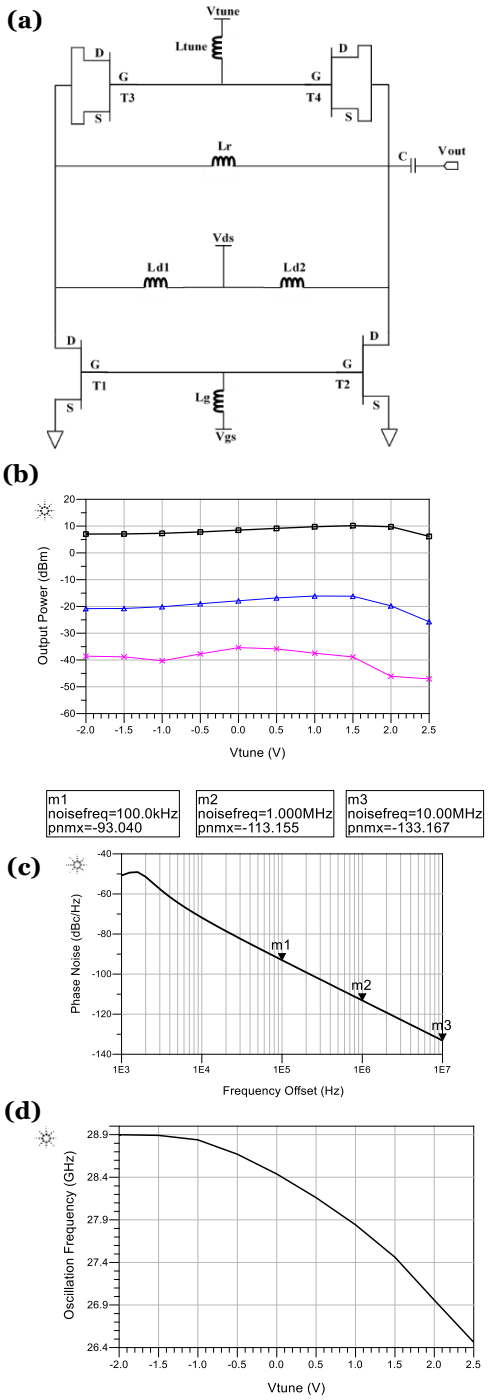


Figure 6. (a) VCO circuit, (b) Output powers versus Vtune, (c) Phase noise, and (d) Oscillation frequency versus Vtune

On the other hand, the power consumption on wireless communication systems is an important challenge (Gures *et. al.,* 2020; Tengku Mohamad *et al.,* 2019). A DC simulation allowed estimating the global consumption of the circuit. The simulation shows that the power consumption of our circuit is about 129 mW.

Finally, Table 3 shows the operation frequency as well as the conversion gain of several SOMs from the literature. As

is shown in table, our circuit presents the highest conversion gain compared to the other published structures.

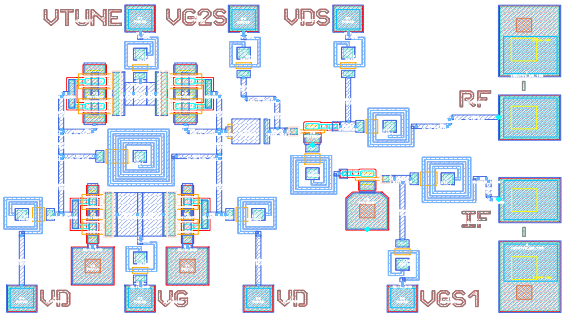


Figure 7. 5G mm-wave Self-oscillating Mixer Layout

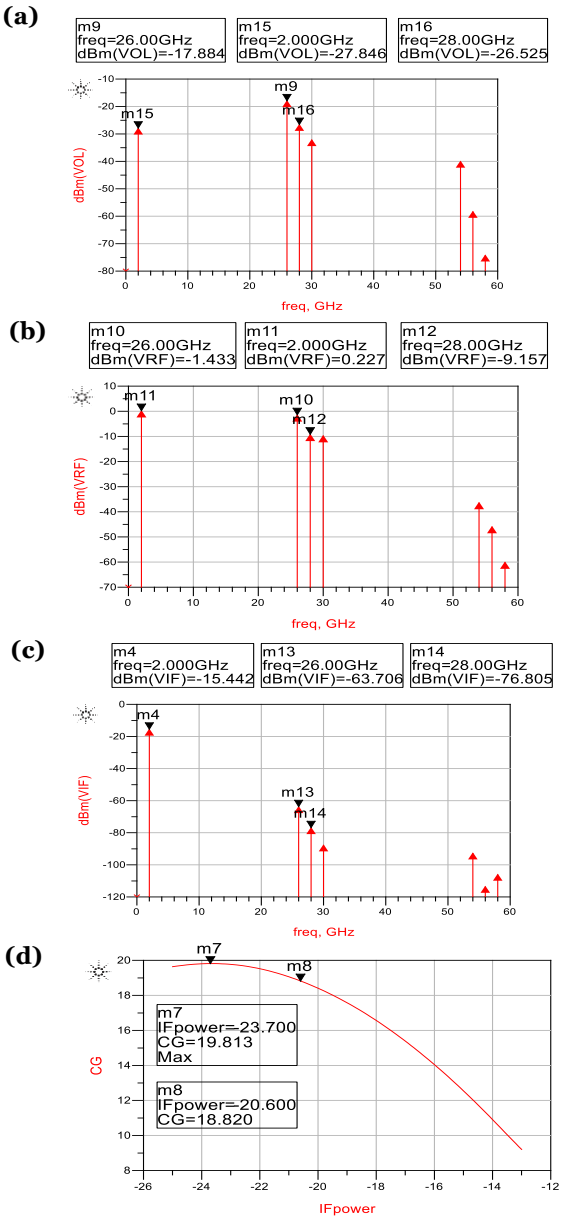


Figure 8. (a), (b) and (c): Power spectrum present at the three ports of the SOM, and (d): conversion gain

V. CONCLUSION

In this paper we presented the design steps of a self-oscillating mixer for 5G applications. The SMO presented has a very high conversion gain of 19.8 dB, the compression point at 1 dB is obtained for an IF power value of -20.6 dBm and occupies a reduced space of 0.741 mm². The circuit is based on the pHEMT transistor using the PH15 technology of UMS foundry.

Table 2. Isolations values between different accesses

Isolation (dB)	-IF	-LO	-RF
IF-to-		12.44	-15
LO-to-	50.3		-17.4
RF-to-	62.3	16.48	

Table 3. Performance summary and comparison of SOMs

	Tech	RF freq (GHz)	CG (dB)	Chip size (mm²)
This work	0.15µm pHEMT	26	19	0. 741
Burasa *et al.*, 2016	65nm CMOS	40	-30	0.24
Kim & Choi, 2010	0.13µm CMOS	30	-30	NA
Adhikary *et al.*, 2017	0.20µm pHEMT	10	-19	NA

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