ASM Sc. J., 17, 2022

https://doi.org/10.32802/asmscj.2022.1224

# Review of Efficiency CMOS Class AB Power Amplifier Topology in Gigahertz Frequencies

R. Sapawi[1*], D.A. Sa' Ahmad[1], K. Hong Ping[1], N. Julai[1], K. Kipli[1], M. Sawawi[2], S. M. W. Masra[1] and Sohiful A.Z. Murad[3]

[1]*Department of Electrical and Electronics Engineering, Universiti Malaysia Sarawak, Jalan Datuk Mohammad Musa, 94300 Kota Samarahan, Sarawak, Malaysia*

.[2]*Department of Mechanical Engineering, Universiti Malaysia Sarawak, Jalan Datuk Mohammad Musa, 94300 Kota Samarahan, Sarawak, Malaysia*

[3]*School of Microelectronic Engineering, Universiti Malaysia Perlis, Kangar, Perlis, Malaysia*

This paper reviewed the efficiency of CMOS class AB power amplifier topology especially in gigahertz frequencies. CMOS class AB power amplifier is a compromise between class A and class B in terms of linearity and efficiency between 50% to 78.5%. However, CMOS class AB power amplifier cannot have good linearity and efficiency simultaneously due to the breakdown in gate-oxide voltage and effects from hot carrier. The breakdown of oxide prevents optimum drain signal and the effect from hot carrier will reduce the quality of the overall PA design. Several works from year 1999 to 2019 with different topology such as multiple gated transistor, cascode, feedforward linearization, differential circuit, transformer combining method with common source harmonic termination and combination of a dual-switching transistor with a third harmonic tuning technique are discussed and the performances of the power amplifier are compared. The best three CMOS class AB power amplifier topologies were chosen in terms of high efficiency. The topologies are two stages with integrated input and interstage matching, Doherty amplifier combined with drain modulation based architectures and self-biased cascode topology that obtained power added efficiency of 45%, 43% and 42%, respectively. Key performance indicators for class AB power amplifier include frequency, power added efficiency, gain and output power are also discussed in this paper.

**Keywords:** power amplifier; CMOS class AB; topology; frequency; power added efficiency; gain

## I. INTRODUCTION

Power amplifier (PA) acts as a crucial part of a transmitter in a radio frequency (RF) transceiver. While PA helps to amplify the signal power high enough for its propagation and need highly efficiency as it becomes a very power-hungry block that takes 50~80% of the total power consumption. PA can be classified into several classes either a linear (class A, B, C, AB) or non-linear switching gates (class D, E, F). The linear power amplifier has excellent linearity with typical efficiency achieved for class A is 25%, class AB is 35-60%, class B is 60% and class C is70%. For non-linear switching the typically maximum efficiency can be achieved is 100%. Main characteristics of the PA design are linearity, efficiency, gain and output power. Due to different performances in each PA classes, there will always be a trade-off between linearity and efficiency.

Linear switching PAs such as PA of class A and B operates based on their load-line curve. This curve shows the optimum voltage supply and current needed to enable the load receives maximum power from the transistor in the circuit design. Biasing condition refers to the electricity flow in the transistor of the amplifier. Class A is biased at the load line's centre causing the transistor to be fully active (ON) and conducts at $180^0$ of the operating signal. Class A has the highest linearity yet least efficiency among other PA classes. Meanwhile, class B has a push pull operation between the transistors where it is not being biased within range of ± 0.7 V causing it to

*Corresponding author's e-mail: srohana@unimas.my

continuously switches ON and OFF at 360⁰. The voltage of ± 0.7 V is chosen because of the threshold voltage of silicon transistor. Although the linearity of class B PA is less than in class A, the configuration of class B produces less distortion compared to class A (Jose, 2004). This resulting in a new type of PA known as class AB where class AB combines both advantages of class A and B. The transistor in class AB conducts individually. It has a small voltage biasing yet large current output, causing the conduction angle is between 180⁰ and 360⁰. Depending on the pre-biasing of the transistors. This leads to higher efficiency than class A and eliminates more cross-over distortion in class B. The harmonics in class AB are also well-controlled to get the best performance of the PA. Example of the basic class AB circuit design and the operating signal can be referred from Figure 1 (Aspencore, 2020).

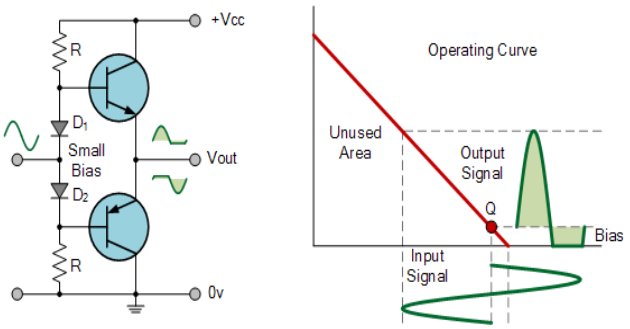


Figure 1. Example of basic class AB circuit and its operating signal (Aspencore, 2020)

There are abundance of research papers available for PA designs with different classes, frequencies and topologies where each paper has its own specialty being presented. There are many topologies used in this paper such as multiple gated transistor (Hang *et al.,* 2011), cascode (Sowlati & Leenaerts, 2002; Solar *et al.,* 2006), feedforward linearization (Liao *et al.,* 2008), differential circuit (Eo & Lee, 2004), transformer combining method with common source harmonic termination (Kang *et. al.,* 2006; Kim *et al.,* 2012), and combination of a dual-switching transistor (DST) with a third harmonic tuning technique (Eswaran *et al.,* 2019). These topologies are discussed and compared for the performances of the PA. This papers are very helpful for the researcher that may takes too much time to gather all the papers according to the desired research topic. This study may help to minimise the scope of finding by chronologically summarised the implementation of CMOS class AB PA designs in GHz frequencies from year 1999 to 2019. The review of the efficiency of class AB PA is presented in the following sections:Section 2 will explain the details of the proposed PA designs. Section 3 will discuss the summary from the findings and Section 4 will conclude the findings.

## II. DESIGN IMPLEMENTATION

Active device (transistor) and passive components such as capacitors, resistors and inductors play a significant role in any RF PA design. The components are carefully selected. These elements will determine the biasing points, load resistance and the output power as well as to get the maximum performance of the PA circuit (Giannini *et. al.*, 2017; Leuzzi *et. al.*, 2017; Limiti *et. al.*, 2017; Scucchia *et al.*, 2017). In class AB, the active device usually been biased close to the pinch-off of the circuit (Giannini *et al.*, 1995). The linearity in class AB PA design is denoted by gain, S21 while the efficiency is denoted by the achieved power added efficiency (PAE). Therefore, throughout the years, different architectural designs, efficiency and linearization techniques are introduced and implemented in designing the CMOS Class AB PA circuit.

Class AB is first being implemented in a RF circuit design by Ballweber *et al.* (1999) where the traditional inductor is replaced with a PMOS transistor. A four-stages class AB circuit is employed by combining bridged T-coil and on-chip spiral inductors in the input matching. The measured results show that gain of 6.5dB±1.2dB, and power dissipation of 83.4 mW are achieved. High PAE of 30% is achieved by increasing the signal current to enchance the $g_m$ that minimise the impact of reduced voltage swing. However, this topology achieved low gain due to four-stage distributed topology that combined with inductors and (parasitic) capacitances act to form L-C transmission line structures.

In year 2000, Giry *et al.* (2000) implemented a single-ended two-stage common source (CS) transistor for 1.9 GHz CMOS class AB PA design as shown in Figure 2. The driver and output stages include the reactive matching networks to provide gain and improve efficiency through inductor L1 and capacitors C1, C2 and C3. This proposed design achieved as high as 23.5 dBm of output power (Pout), 24.6 dB of gain while PAE obtained is around 35%. Compare to study by

Ballweber *et al.* (1999), this topology provides a good trade-off between linearity and efficiency and suitable for short range RF applications around 2 GHz requiring linear medium power amplification.

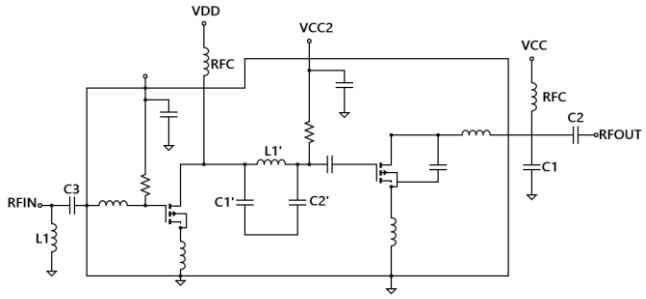


Figure 2. Schematic circuit of class AB (Giry *et al.,* 2000)

A 0.35 µm CMOS class AB PA was proposed by (Fallesen & Asbeck, 2001). Class AB operation was chosen by considering its linear relativity, effectiveness and ability to provide sufficient gate-oxide for the amplifier. As shown in Figure 3 an inductor-capacitor, LC network was implemented in matching input/output networks and the inter-stage of the circuit where it helps in blocking and biasing the current as well as harmonics termination. With the frequency of 1.75 GHz, the highest PAE achieved is 45% with Pout of 30.4 dBm. However, the gain measurement was not included in the results and large area of 1.9mm² was achieved. Based on the results, this topology design is suitable for digital predistortion.

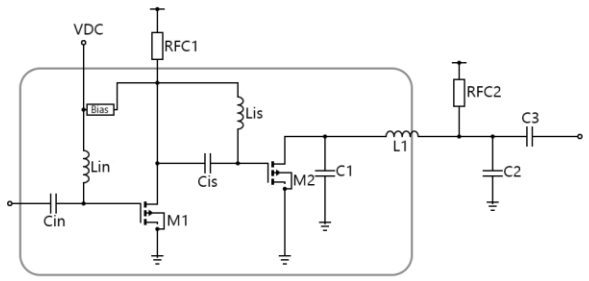


Figure 3. Proposed 1.75 GHz PA design (Fallesen & Asbeck, 2001)

Later, a two-stage 0.18 µm CMOS class AB PA was implemented in (Sowlati & Leenaerts, 2002) as depicted in Figure 4. A cascode topology is applied in both stages of the circuit. Self-biased condition s when two transistors are connected in parallel where common source (CS) transistor is placed below the common gate (CG) transistor. This is shown through M1 and M3 as CS transistors while transistors M2 and M4 as CG transistors. C1 and C5 capacitors act as dc blocking while transmission lines TL1 to TL7 as driver and power stages as well as the harmonic termination in the circuit. The gain of 31 dB, and Pout of 23 dBm were achieved. The advantage of using self-biased cascode topology compared to conventional cascode topology is reduce the hot carrier effects. High PAE is achieved by using sliding bias technique on both stages to enhance the PAE at low/mid-power levels and the gain variation can be reduced significantly. With this characteristic the topology fulfils the Bluetooth Class-1 requirements.

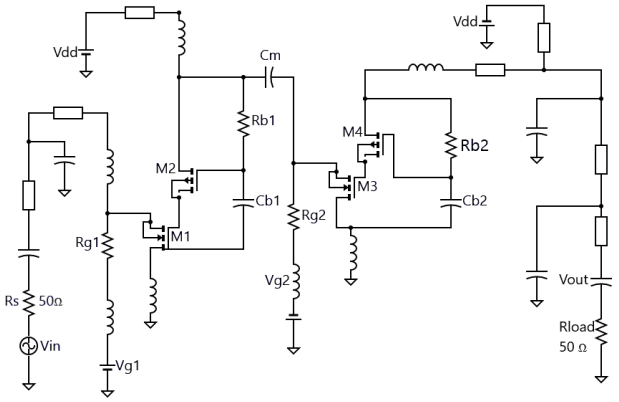


Figure 4. Schematic circuit of proposed PA (Sowlati & Leenaerts, 2002)

In 2003, a single stage 2.45 GHz class AB PA was proposed for Bluetooth/ISM applications (Khannur, 2003). As shown in Figure 5, with only 1.8V of supply voltage, resistor R1 and capacitor C3 ensure the stability of the circuit. The input matching is obtained from the combination of C1, C2 and L1 while the output matching circuit is achieved from the combination of C4, C5 and L3. A large parameter of transistor M2 is chosen to minimise the power supply's voltage drop. The proposed design achieved a low $P_{out}$ which only 3.5 dBm with PAE of 12.0% while the gain measurement was not specified.

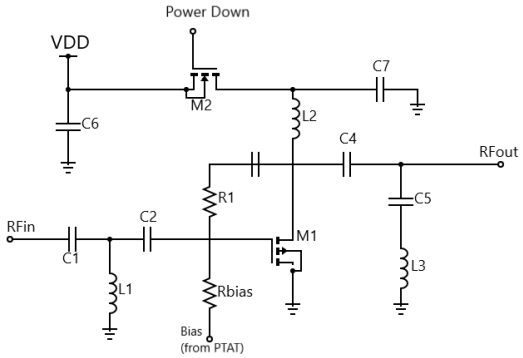


Figure 5. Single stage class AB of 2.45 GHz PA (Khannur, 2003)

A 1.92 GHz class AB 0.13 µm CMOS PA was proposed to match wireless sensor applications (Chee *et al.*, 2004). By referring to Figure 6, Class AB is very suitable in this design as it only needs two transmit power compared to switching PAs. A maximum efficiency is delivered by using cascoded transistors, M1 and M2 together with capacitive transformers, C1 and C2 in the matching networks. This design obtained 26% of PAE due to capacitive transformer is employed to match the antenna to PA for maximum efficiency and reduce impedance loss. However, the gain and output power achieved are quite low which is 6 dB and 3 dBm, respectively and this topology is suitable for ad-hoc wireless sensor network.

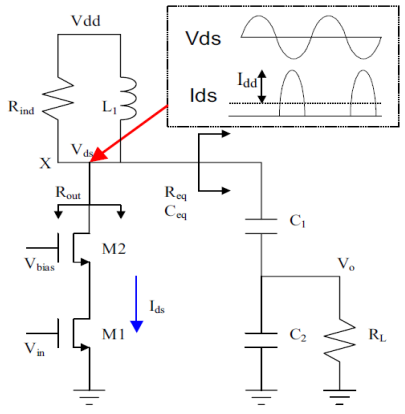


Figure 6. Cascode topology with capacitive transformer (Chee *et al.*, 2004)

Figure 7 shows the schematic circuit for a 5 GHz using 0.18µm CMOS PA with topology of three-stage differential transistors with matching networks presented in (Eo & Lee, 2004). The driver stages implemented resistor shunt feedback while a shunt bias feed resistor is in the last PA stage. This work achieved high linearity, gain of 21 dB, Pout of 21.8 dBm and PAE of 13.1%. The drawback of using the three-stage differential, it deteriorates the efficiency in order to achieve desired gain more than 20 dB. Moreover, it consumed more power compared to other topology i.e., 1150mW and large die size of 1.8mm².

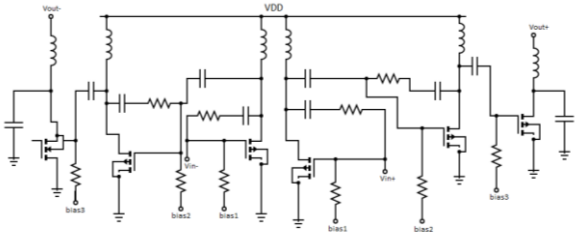


Figure 7. Differential Three-stage PA design (Eo & Lee, 2004)

A two-stage CMOS PA was proposed by Abdelsayed *et al.* (2005) and Kang *et al.* (2005). Figure 8 shows the proposed fully on-chip 2.45 GHz for biomedical applications (Abdelsayed *et al.*, 2005). Class AB operation was selected as it only needs a small driver input while providing good linearity and less power consumption. Two-stage cascode configuration aids to boost the efficiency of the circuit. This design achieved PAE of 28.5% and gain of 19.5 dB. Although the Pout is only 6.53 dBm, it matched the requirement for low-power biomedical implanted transceiver systems. The efficiency of PA degraded due to poor quality of the inductors that has low resistivity in silicon substrate CMOS process. Meanwhile, the proposed PA by Kang *et al.* (2005) proves the need of more number of harmonic termination for linearity improvement especially when it occurs in CS region. The advantage of second harmonic termination at the common source technique demonstrates excellent on linearity without reducing output power and PAE across a broad power range.

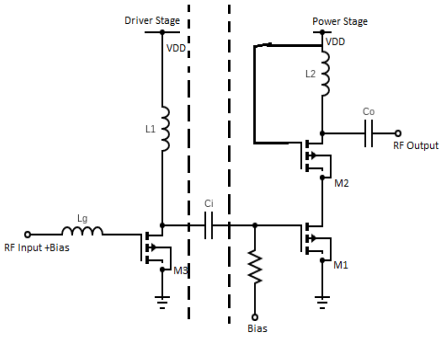


Figure 8. Proposed PA circuit for biomedical applications (Abdelsayed *et al.*, 2005)

Three different PA designs with two-stage transistors were proposed in year 2006 (Kang *et. al.,* 2006; Solar *et al.,* 2006). A new CS harmonic termination applied by Kang *et al.* (2006). The PA design established a high efficiency and linearity as it achieved PAE of 37% and gain of 17.5 dB and Pout of 20.5 dBm. Then, a single chip self-biased 0.18µm CMOS PA was proposed by Kang *et al.* (2006). A deep N-well in the NMOS transistor aid in terminating the 2nd and 3rd harmonics thus, reducing the nonlinearity of the circuit. A 24.5 dBm of Pout, 31% of PAE and 19.8 dB of gain are delivered from the circuit. This topology is suitable for 2.4GHz WLAN for IEEE 802.11g standard. Meanwhile, Figure 9 shows the schematic circuit of PA design by Solar *et al.* (2006). This work proposed a implemented an equal size of transistors with cascode topology to 'power inductors' concept to improve the linearity and achieve good gain. With PAE of 26.7%, power gain of 25.5 dB and Pout of 26.5 dBm were obtained. And this work claimed the highest Pout obtained among high frequency CMOS PA that suitable for 5-GHz WLAN applications.

Another PA design of high frequency wireless application was presented in (Tu & Chen, 2007) with two-stage self-biasing and an off-chip output matching network. The differential cascode configuration allows harmonics termination and reduce the distortion. This PA only achieved 20 dBm of Pout and 20% of PAE. This topology was designed to improve the linearity of 18.8 dBm by using a transistor-level compensation voltage and the hot carrier degradation without degrading the PAE.

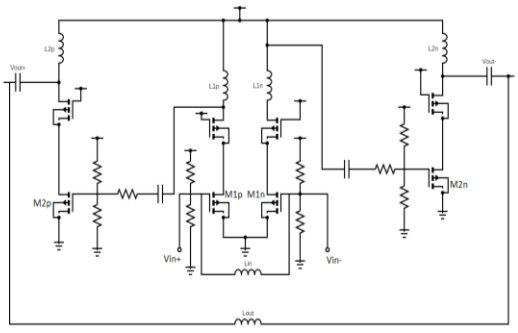


Figure 9. Schematic circuit with 'power inductors' concept (Solar *et al.,* 2006)

Since linearity and efficiency determine the overall performance of a PA, several works focused on the enhancement for both criteria (Liao *et. al.,* 2008; Liu *et al.,* 2008). Referring to Figure 10, a feedforward linearisation architecture was implemented in two-stage topology noted as (M1, M2) and (M5, M6) as the main and error amplifiers to achieve satisfying gain and PAE (Liao *et al.,* 2008). The stability of the circuit was maintained by sets of (R1 & R2) and (C1 & C2) while a high-pass and low-pass type of matching are used for DC blocking and harmonic suppression. At 2.6 GHz, this circuit able to conduct at 240 degrees and obtained PAE of 26.6%, gain of 12.3 dB and Pout of 22.1 dBm. The advantage of feedforward linearization technique is the linearization bandwidth and cancellation performance that suitable for high linear PA design and WiMAX communication system, where linearity of PA is more significant than the efficiency. Then, Figure 11 illustrates the circuit of a pseudo-differential cascode single-ended PA presented by Liu *et al.* (2008). An equivalent size of transistors M1 and M2 enable efficiency and reliability improvement. This PA achieved Pout of 24 dBm. However, the power gain is unknown because the input is not matched. Moreover, the results of the gain and PAE are not stated in this paper but the efficiency at power back-off showed significant improvement which employs average efficiency enhancement circuitry by using voltage combining transformers technique.

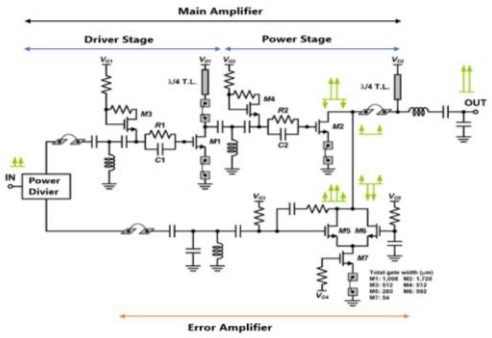


Figure 10. Proposed PA circuit with feedforward technique (Liao *et al.,* 2008)

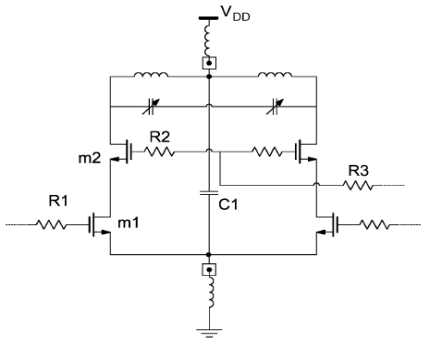


Figure 11. Proposed pseudo-differential schematic design (Liu *et al.,* 2008)

More research works on class AB CMOS PA for wireless applications were published by (An *et. al.,* 2009; Chowdhury *et. al.*, 2009; Haridas, *et. al*, 2009; Qian *et al.,* 2009). Transformer combining method is applied by Laskar *et al.* (2009) and Chowdury *et al.* (2009) to increase the overall power and efficiency. Voltage stress on CMOS devices were prevented by using CS and CG transistors through cascode configuration. A dual band PA was proposed in (Ghajar, 2009) where the matching networks were stacked in parallel allowing the components to turn into either resonator or inductor/capacitor at other frequency. This PA achieved high efficiency drain modulation using Doherty amplifier technique. However, Doherty amplifier technique is not appropriate for multiband and multi-standard operation as it achieves high efficiency over narrow frequency band.

Figure 12(a) shows the proposed circuit at 2.4 GHz and 3.5 GHz while Figure 12(b) and (c) shows the simplified circuit for both frequencies (Ghajar, 2009). The π matching network was represented by the combination of C3, C4 and L which turns to load/drain impedance. C1b and L1b act as a capacitor at 2.4 GHz while L2 and C2 act as an inductor at 3.5 GHz for the circuit output matching. Both frequencies achieved PAE of 48%. However, no measurement for the gain and output power was reported.

A new linearization technique known as multiple gated transistor (MGTR) and parallel-series combining transistor (PSCT) were employed by Kornegay *et al.* (2012) and Park *et al.* (2014). MGTR technique is preferable for high frequency PA design as large input is required. PSCT benefits in improving the limitations of other transformer combining techniques. Apart from common audio PA, Class AB is also suitable for healthcare sensor application (Wei *et al.,* 2016). Driver and power stages are optimised to provide good gain and low output power to the overall circuit. Although only gain of 10 dB and PAE of 7.5% are achieved, this PA transmit Pout 21.3 of dBm which achieved the design target and this design focus on linearity compared to PAE. More studies on class AB PA design can be referred in (Choudhary *et. al.,* 2017; Eswaran *et. al.,* 2014; Kurniawan *et. al.,* 2019; Giannini *et. al.,* 1995; Albulet, 2001).

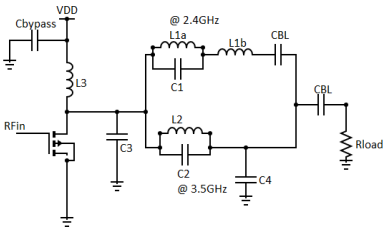


Figure 12(a). Circuit of dual band PA (Ghajar, 2009)

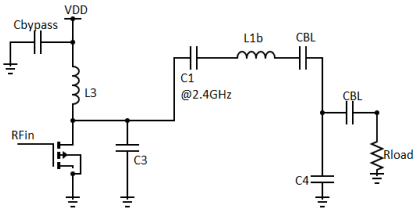


Figure 12(b). Simplified circuit at 2.4 GHz (Ghajar, 2009)

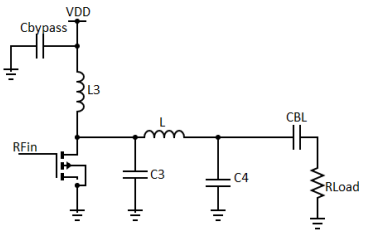


Figure 12(c). Simplified circuit at 3.5 GHz (Ghajar, 2009)

## III. SUMMARY

Class AB is an effective power amplifier that has high linearity with moderate output power among other linear switching PAs. In general, class AB PA able to achieve as high as 78.5% of efficiency. Several techniques are introduced to be implemented with CMOS class AB PA in order to achieve high efficiency and linearity. Among the techniques are multiple gated transistor, cascode, feedforward linearization, differential circuit, transformer combining method with

common source harmonic termination and combination of a dual-switching transistor with a third harmonic tuning technique.. Also, CMOS technology for wireless applications give advantage to increase in efficiency as well as low cost. However, CMOS class AB PA cannot have good linearity and efficiency simultaneously due to the breakdown in gate-oxide voltage and effects from hot carrier. The breakdown of oxide prevents optimum drain signal while the affect from hot carrier reduces the quality of the overall PA design. Therefore, cascode stage is preferable for PA design where a thin oxide transistor (CS) is placed above a thick oxide transistor (CG). This configuration alleviates the deficiency in CMOS PA. Nevertheless, class AB produces high harmonic current at the final transistor. This resulting in inadequate load impedance which degrades the PA performance. Therefore, suitable biasing and linearization technique and optimised components performances for the PA circuit is a challenge to design a highly linear and efficiency class AB PA.

A comparison of class AB performances are presented in Table 1. From Table 1, the highest PAE is 45% with two stages that integrated input and interstage matching topology, followed by Doherty amplifier and drain modulation based architectures with PAE of 43% and self-biased cascode topology with PAE of 42%. Doherty is considered to be ahead of the other as it can offer better efficiency than outphasing. The latest technique used in designing CMOS Class AB PA is dual-switching transistor with third harmonic tuning technique that achieved high linearity and high PAE of 34.5% using 0.18 μm CMOS technology. Theoretically, CMOS class AB PA can reached as maximum as 78.5% of efficiency with high linearity. However, none of the published papers that discussed in here achieved efficiency of 78.5% due to the PA is power hungry component that consume total power consumption of 50~80%. Furthermore, typically CMOS class AB PA can achieved efficiency of 35-60% (Sapawi, R. 2017) compared to published PA design that achieved PAE of 12-45%. It shows that the published PA designs are within the range except for Khannur (2003) due to the single stage class AB topology used that not only effect the PAE but also the gain of 3.5 dB. Mostly, CMOS class AB Power amplifiers are designed based on the specification and application to achieve the desired outcome. Therefore, Table 1 shows that CMOS Class AB PA has different of design, technology, results such as efficiency, gain, frequency, and output power in order to achieve desired outcome and specification based on the system application.

Table 1. Comparison performances of class AB PA

| Ref | Tech m | Freq GHz | Gain dB | PAE % | Pout dBm | Topology |
|---|---|---|---|---|---|---|
| Ballweber *et al.,* 1999 | 0.6μ | 0.5-5.3 | 6.5 ±1.2 | 30 | - | Four-stage distributed CMOS |
| Giry *et al.,* 2000 | 0.35μ | 1.9 | 24.6 | 35.0 | 23.5 | Single-ended 2-stage common source amplifier |
| Fallesen & Asbeck, 2000 | 0.35μ | 1.7 | - | 45.0 | 30.4 | Two stages with integrated input and interstage matching. |
| Sowlati & Leenaerts, 2002 | 0.35μ | 2.4 | 31.0 | 42.0 | 23.0 | Self-Biased Cascode Topology |
| Khannur, 2003 | 0.18μ | 2.45 | - | 12.0 | 3.5 | Single stage class AB |
| Chee *et al.,* 2004 | 0.13μ | 1.92 | 6 | 26.0 | 3 | Cascode topology with capacitive transformer |
| Eo & Lee, 2004 | 0.18μ | 5.0 | 21 | 13.0 | 24.1 | Differential three-stage amplifiers |

| | | | | | | |
|---|---|---|---|---|---|---|
| Abdelsayed *et al.,* 2005 | 0.18µ | 2.45 | 19.5 | 28.5 | 6.53 | Two-stage PA circuit and interstage matching networks |
| Kang *et al.,* 2005 | 0.18µ | 2.45 | 17.5 | 37.0 | 20.5 | Fully differential and harmonic termination technique |
| Kang *et al.,* 2006 | 0.18µ | 2.45 | 17.5 | 37.0 | 20.5 | Two-stage circuit and harmonic termination technique |
| Kang *et al.,* 2006 | 0.18µ | 2.4 | - | 31.0 | 24.5 | Fully differential topology with transformer |
| Solar *et al.,* 2006 | 0.18µ | 5.0 | 25.5 | 26.7 | 26.5 | Two stages in a cascode differential configuration. |
| Tu & Chen, 2007 | 0.35µ | 5.25 | - | 20.1 | 20 | Two gain stage structure and off chip output matching circuit |
| Liao *et al.,* 2008 | 0.18µ | 2.6 | 12.3 | 26.6 | 22.1 | Feedforward linearization technique power amplifier |
| Liu *et al.,* 2008 | 0.13µ | 2.4 | 20.0 | - | 27 | Transformer based voltage combiner |
| An *et al.,* 2009 | 0.18µ | 2.4 | >20 | 27 | 31 | Parallel-combining transformer (PCT) and gate bias adaptation |
| Chowdhury *et al.,* 2009 | 90n | 2.4 | 28 | 12.4 | 22.7 | Two-stage transformer-based power combiner |
| M. R. Ghajar, 2009 | 0.13µ | 2.4 and 3.5 | - | 43.0 | - | Doherty amplifier and drain modulation based architectures |
| Haridas *et al.,* 2009 | 0.18µ | 2.45 | - | 18.0 | 6.4 | Differential power amplifier |
| Mingfu Zhao *et al.,* 2009 | 0.18µ | 2.45 | 22.5 | 37.0 | 23.5 | Two-stage architecture and off-chip output matching network. |
| Qian *et al.,* 2009 | 0.18µ | 2.4 | 20.6 | 21.2 | 24.8 | Two-stage differential structure |
| Wang *et al.,* 2010 | 90n | 5.2 – 13.0 | 18.5 | 21.6 | 25.2 | Differential PA |
| H. Liu *et al.,* 2011 | 0.18µ | 5.2 | 15.8 | 32.87 | 26.18 | Multiple Gated Transistor Technique |
| Kim *et al.,* 2012 | 0.18µ | 2.4 | 22.0 | 34.9 | 23.5 | Parallel-Series Combining Transformer |
| Park *et al.,* 2014 | 0.18µ | 1.85 | - | 36.5 | 27 | Envelope Tracking Operation |

| | | | | | | |
|---|---|---|---|---|---|---|
| Gadallah *et al.,* 2015 | 0.18µ | 3 - 7 | 12 ± 0.8 | 38.5 | 7.21 | Source and Load-pull contours |
| Kim *et al.,* 2015 | - | 1.7 – 2.0 | - | 38.6 – 35.1 | 26.5 | Adaptive bias circuit, harmonic control, and dynamic auxiliary circuits |
| Ye *et al.,* 2015 | 65n | 2.0 – 6.0 | 23.6±0.8 | 28.4 | 9.31 - 11.31 | Output matching technique based on differential architecture |
| Ryu, 2015 | 0.18µ | 2.4 | - | 41.7 | 22 | Dual gate bias |
| Wei *et al.,* 2016 | 0.18µ | 2.4 | 10.0 | 7.5 | 10 | Two stage common source amplifiers |
| Choudhary *et al.,* 2017 | 90n | 2.5 | 33.4 | 29.0 | - | Parallel cascade class A&B power amplifier is used. |
| Eswaran *et al.,* 2019 | 0.18µ | 2.5 | 11.0 | 34.5 | 10.1 | Dual-switching transistor (DST) with third harmonic tuning technique |

## IV. CONCLUSION

Review effciency of CMOS class AB power amplifier designs in Gigahertz frequencies from year 1999 to 2019 has been presented. CMOS Class AB PA offers different architecture designs for instance cascode, self-biased cascode, differential cascode and parallel series power combining transformer. Among these topologies, the best three CMOS class AB power amplifier topologies in term of high efficiency are two stages with integrated input and interstage matching, Doherty amplifier combined with drain modulation based architectures and self-biased cascode topology that obtained power added efficiency of 45%, 43% and 42%, respectively. The parameters and topology must be carefully selected to enable class AB PA with CMOS technology to perform as maximum as possible. Thus, the authors believe that CMOS class AB PA has good potential in achieving high efficiency and linearity for the upcoming wireless RF application.

## V. ACKNOWLEDGEMENT

The author would like to thank Ministry of Higher Education, Malaysia, Fundamental Research Grant Scheme (FRGS/1/2020/TK0/UNIMAS/02/6) and Universiti Malaysia Sarawak (F02/FRGS/2005/2020) for supporting this work.

## V. REFERENCES

Abdelsayed, MJD & Nikolova 2005, 'A Fully Integrated Low-Power CMOS Power Amplifier for Biomedical Applications', European Microwave Conference, pp. 17-18.

Albulet 2001, 'RF Power Amplifiers', Atlanta: Noble Publishing Corporation, pp. 1-3'.

An, DHL & OL, Kim, Han, WK & CHL, HK & Laskar 2009, 'A 2.4 GHz Fully Integrated Linear CMOS Power Amplifier with Discrete Power Control', IEEE Microwave and Wireless Components Letters, vol. 19, no. 7, pp. 479–481.

Aspencore Inc. 2020, 'Electronics Tutorial: Amplifier Classes.

Ballweber, Gupta & Allstot 1999, 'Fully-Integrated CMOS RF Amplifiers', IEEE international Solid-state Circuits Conference, pp. 72-74.

Bhuiyan, MTIB & MBIR 2019, 'Design Architectures of the CMOS Power Amplifier for 2.4 GHz ISM Band Applications: An Overview', MDPI Journal (Electronics), vol. 8, no. 477, pp. 1-21.

Chee, JR & Niknejad, 2004, 'A Class AB Low Power Amplifier for Wireless Sensor Networks', International Symposium on Circuits and Systems (ISCAS), pp. 409–412.

Chen, SHL & Tu 2007, 'A 5.25-GHz CMOS Cascode Class-AB Power Amplifier for Wireless Communication', IEEE Conference on Electron Devices and Solid-State Circuits, pp. 421–424.

Choudhary, Karawal & Ranjan 2017, 'Linear CMOS Power Amplifier for WiMAX Application', International Research Journal of Engineering and Technology (IRJET), vol. 4, no. 6, pp. 1657–1660.

Chowdhury, CDH & OBD, Wang & Niknejad 2009, 'A Fully Integrated Dual-Mode Highly Linear 2.4 GHz CMOS Power Amplifier for 4G WiMax Applications', IEEE Journal of Solid-State Circuits, vol. 44, no. 12, pp. 3393–3402.

Cripps 2003, 'Advanced techniques in RF power amplifier design', Boston, MA: Artech House, pp. 1-9.

Cripps 2006, 'RF power amplifiers for wireless communications', 2nd ed. Boston: Artech House, pp. 67-89.

Eo, KL 2004, 'A Fully Integrated 24-dBm CMOS Power Amplifier for 802.11a WLAN Applications', IEEE Microwave and Wireless Components Letters, vol. 14, no. 11, pp. 504–506.

Eswaran, HR & JK 2014, 'Power Amplifier Design Methodologies for Next Generation Wireless Communications', IETE Technical Review, vol. 31, no. 3, pp. 241-248.

Fallesen, PA 2001, 'A 1W 0.35µm CMOS Power Amplifier for GSM-1800 with 45% PAE', IEEE MTT-S International Microwave Symposium Digest 1, pp. 493 – 496.

Gadallah, AA & HM, Abdel-Rahman, Jia & Pokharel 2015, 'A High Efficiency 3-7 GHz Class AB CMOS Power Amplifier for WBAN Applications', IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), pp. 163–165.

Ghajar, 2009, 'High Efficiency CMOS Power Amplifiers for Drain Modulation Based RF Transmitters', Dissertation, pp. 1-10.

Giannini, GL & EL 1995, 'Class AB Power Amplifier Advanced Design Techniques', Microwave and Optoelectronics Conference Proceedings, pp. 361-368.

Giannini, Leuzzi & Limiti 1995, 'Class AB power amplifier advanced design techniques', Proceedings of SBMO, IEEE MTT-S International Microwave and Optoelectronics Conference, pp. 361–368.

Giannini, Leuzzi, Limiti & Scucchia 1993, 'Class-AB Power Amplifier Design Guidelines', SBMO International Microwave Conference, Brazil, pp. 187–192.

Giry, JM & Pons 2000, 'A 1.9 GHz Low Voltage CMOS Power Amplifier for Medium Power RF Applications', IEEE Radio Frequency Integrated Circuits (RFIC) Symposium Digest of Papers, pp. 121-124.

Hajimiri, JK & Kim 2006, 'A Single-Chip Linear CMOS Power Amplifier for 2.4 GHz WLAN', IEEE International Solid-State Circuits Conference - Digest of Technical Papers, pp. 761-769.

Haridas, TT & XY 2009, 'A 2.4-GHz CMOS Power Amplifier Design for Low Power Wireless Sensors Network', IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), pp. 299–302.

Jose, S 2004, 'Design of RF CMOS Power Amplifier for UWB Applications', MSc in Electrical Engineering: Virginia Polytechnic Institute and State University, Virginia, pp. 13-14.

Kang, JY & KM, Yu, JN & YY 2006, 'A Highly Linear and Efficient Differential CMOS Power Amplifier with Harmonic Control', IEEE Journal of Solid-State Circuits, vol. 41, no. 6, pp. 1314–1322.

Kang, KL & JY, Chung, SH & BK 2005, 'Differential CMOS Linear Power Amplifier with 2nd Harmonic Termination at Common Source Node', Radio Frequency Integrated Circuits (RFIC) Symposium: Digest of Papers, pp. 443-446.

Khannur 2003, 'A CMOS Power Amplifier with Power Control and T/R Switch for 2.45-GHz Bluetooth/ISM Band Applications', IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 145–148.

Kim, BP & SJ 2015, 'Design of an Advanced CMOS Power Amplifier (Invited Paper)', Journal of Electromagnetic engineering and Science, vol. 15, no. 2, pp. 63–75.

Kim, WK & HJ, Huang, Yoon, Kim, Lee and Kornegay 2012, 'A Fully-Integrated High-Power Linear CMOS Power Amplifier with a Parallel-Series Combining Transformer', IEEE Journal of Solid-State Circuits, vol. 47, no. 3, pp. 599–614.

Kurniawan, Yoshimasu 2019, 'A 2.5-GHz 1-V High Efficiency CMOS Power Amplifier IC with a Dual-Switching Transistor and Third Harmonic Tuning Technique', MDPI Journal (Electronics), vol. 8, no. 69, pp. 1-15.

Liao, JHC & HKC & Chen 2008, 'High-Linearity CMOS Feedforward Power Amplifier for WiMAX Application', Asia-Pacific Microwave Conference, pp. 1-4.

Liu, CCB & MAD & Yeo 2011, 'Design and Analysis of a WLAN CMOS Power Amplifier Using Multiple Gated Transistor Technique', International Journal of RF and Microwave Computer-Aided Engineering, vol. 21, no. 2, pp. 157–163.

Liu, Haldi, TJKL & Niknejad 2008, 'Fully Integrated CMOS Power Amplifier with Efficiency Enhancement at Power Back-Off', IEEE Journal of Solid-State Circuits, vol. 43, no. 3, pp. 600–609.

Park, Kim, YC & SJ, Kang & Kim 2014, 'CMOS Linear Power Amplifier with Envelope Tracking Operation (Invited Paper)', Journal of Electromagnetic Engineering and Science, vol. 14, no. 1, pp. 1–8.

Qian, WL & ZW 2010, '2.4-GHz 0.18-μm CMOS Highly Linear Power Amplifier', International Conference on Advanced Technologies for Communications, pp. 210–212.

Ryu, 2015, 'Highly Linear Efficient CMOS Power Amplifier Design for 802.11g WLAN Application, PhD dissertation pp. 27-41.

Sapawi 2017, Radio Frequency Wideband Power Amplifiers: Design and Analysis, UNIMAS Publisher, 2017.

Solar, RB & IA, Alvarado, ICendoya 2006, 'A Fully Integrated 26.5 dBm CMOS Power Amplifier for IEEE 802.11a WLAN Standard with on-chip power inductors', IEEE MTT-S International Microwave Symposium Digest

Sowlati, DL 2002, 'A 2.4GHz 0.18μm CMOS Self-Biased Cascode Power Amplifier with 23dBm Output Power,' in: IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 1318-1324.

Wang, CS, Hajimiri 2010, 'A 5.2-to-13GHz class-AB CMOS power amplifier with a 25.2dBm peak output power at 21.6% PAE', IEEE International Solid-State Circuits Conference (ISSCC), pp. 43–45.

Wei, HL & WW 2016, '2.4GHz Class AB Power Amplifier for Healthcare Application', International Journal of Biomedical Engineering and Science (IJBES), vol. 3, no. 2, pp. 1–6.

Ye, KM & KSY 2015, 'A 2-to-6GHz Class-AB Power Amplifier with 28.4% PAE in 65nm CMOS Supporting 256QAM', IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 38–39.

Zhao, LS & JW, Yu & Kang 2009, 'A 2.45GHz CMOS Power Amplifier with High Linearity', IEEE 8th International Conference on ASIC, pp. 383–386.